UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,187	04/22/2004	Charles N. Shaver	200314180-1	6057

22879 7590 07/05/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
SPITTLE, MATTHEW D	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 07/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,187	SHAVER, CHARLES N.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 30 have been examined.

Response to Arguments

Applicant's arguments with respect to claims 1 – 27 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 11 recites the limitation "the computer system" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 4, 5, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lembo in view of Cyberdata Corporation, Carson et al. (US 5,911,051) and Dunlap et al. (US 6,760,799).

Regarding claim 1, Lembo teaches an expansion card (page 2) for adding to a computer system a Universal Serial Bus (USB) port, comprising:

A card connector configured to enable the expansion card to be inserted into an expansion slot of the computer system (Lembo teaches the card having a PCI card connector; pages 1 – 3);

At least one USB port each adapted to mate with a USB-compatible peripheral device (Lembo teaches 4 USB ports; pages 1, 2);

A power connector matable with a corresponding power connector of the computer system, through which a power signal is received and routed to the at least one USB port (Examiner notes that certain elements in the figure of Lembo may be difficult to discern, and so turns to referencing the Operations Manual of Cyberdata Corporation of the same product. Examiner interprets features shown in the Operations Manual to be inherent in the expansion card as shown in Lembo. Page 2, Figure 2 of Cyberdata Corporation shows a power connector on the expansion card matable with a corresponding power connector of a computer system power supply. This power is routed to the USB PlusPower connectors as taught on Page 6 under the section "Power Supply.").

A voltage doubling circuit configured to double the power signal (page 3 of Lembo teaches a "boost converter" to double the 12V power signal to 24V; see note under "Connector Configurations.").

Lembo and Cyberdata Corporation fail to teach wherein the expansion card uses an Accelerated Graphics Port (AGP) card connector.

Carson et al. teaches using an Accelerated Graphics Port (AGP) card for the purpose of increasing performance and efficiency through hiding memory access latency, demultiplexing of address and data on the bus, and AC timing (column 4, lines 1 – 11). The system of Carson et al. relates to using AGP for graphics applications. However, Dunlap et al. teach that AGP can also be used for high-volume network traffic (e.g., USB), as well (column 8, line 66 – column 9, line 2).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate an AGP card connector in the expansion card of Lembo and Cyberdata Corporation for the purpose of improving performance and efficiency.

Regarding claim 2, Cyberdata Corporation teaches the additional limitation wherein one or more of the at least one USB port is a USB Plus-Power port comprising a USB receptacle at which a USB data signal and a USB power signal are presented (page 4, pins 1 – 4, and a power receptacle at which the power signal is presented to the mated USB-compatible peripheral device (page 4, pins 5 – 8).

Regarding claim 4, Lembo teaches the additional limitation wherein the power signal is routed to at least one of the one or more USB-Plus-Power ports (page 2 teaches the four Powered USB connectors are powered directly from the host power supply).

Regarding claim 5, Lembo teaches the additional limitation wherein the power signal is a 12VDC power signal (page 2).

Regarding claim 7, Lembo teaches the additional limitation wherein the voltage doubling circuit converts the 12VDC power signal to a 24VDC power signal (where the doubling circuit is interpreted as a boost converter; page 3, see note under "Connector Configurations.").

Wherein the 24VDC power signal is routed to one or more of the at least one USB-Plus-Power ports (page 3, see "Connector Configurations"; CD#010567A shows Port 1 having the 24VDC power signal).

Regarding claim 8, Lembo teaches the additional limitation wherein the USB power signals are routed to all of the USB-Plus-Power ports (page 2 teaches the four Powered USB connectors are powered directly from the host power supply).

* * *

Claim 3 is rejected under 35 U.S.C. 103(a) as being obvious over Lembo in view of Cyberdata Corporation, Carson et al. (US 5,911,051), Dunlap et al. (US 6,760,799), and further in view of Lelong et al. (US Pub. 2004/0033734).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2). .

With regard to claim 3, Lembo, Cyberdata Corporation, Carson et al., and Dunlap et al. fail to teach a USB connector, matable with a corresponding USB connector of the computer system, at which at least one additional USB data signal and at least one USB power signal generated by the computer system are received, wherein each of the

additional USB data signal and USB power signal is routed to one or more of the at least one USB port.

Lelong et al. teach a USB connector (Figure 2, item 103), matable with a corresponding USB connector of the computer system (Figure 2, labeled "USB header"; Figure 1, item 15), at which at least one additional USB data signal and at least one USB power signal generated by the computer system are received, wherein each of the additional USB data signal and USB power signal is routed to one or more of the at least one USB port (paragraph 39).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the USB connector as taught by Lelong et al. into the expansion card of Intel Corporation. This would have been obvious in order to allow the USB ports provided on the expansion card to be controlled by a USB host controller incorporated into the computer system motherboard, thus making it unnecessary to include the USB host controller on the expansion card, thus reducing its cost.

* * *

Claim 6 is rejected under 35 U.S.C. 103(a) as being obvious over Lembo in view of Cyberdata Corporation, Carson et al. (US 5,911,051), Dunlap et al. (US 6,760,799), and further in view of Espenshade et al. (US 6,685,505).

With regard to claim 6, Lembo, Cyberdata Corporation, Carson et al., and Dunlap et al. fail to teach the expansion card further comprising at least one circuit each

associated with one of the at least one USB port, wherein each circuit performs signal conditioning operations on at least one signal provided at its associated USB port.

Espenshade et al. teach a USB connector that comprises a circuit that performs signal conditioning operations on at least one signal provided at its associated USB port (column 2, lines 9 – 15).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the signal conditioning USB connector of Espenshade et al. in the expansion card of Lembo, Cyberdata Corporation, Carson et al., and Dunlap et al. This would have been obvious since Espenshade et al. teach that the signal conditioning components within their USB connector eliminates undesirable extraneous signals such as high frequency noises (column 4, lines 25 – 28).

* * *

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lembo in view of Cyberdata Corporation, Carson et al. (US 5,911,051), Dunlap et al. (US 6,760,799), and in view of Texas Instruments.

Regarding claim 9, Lembo, Cyberdata Corporation, Carson et al., and Dunlap et al. fail to teach the details of the voltage doubling circuit.

Examiner takes official notice that voltage-doubling circuits are old and well known in this art. This is evidenced by Texas Instruments, where in the TL497A switching voltage regulator specification, an example of an application is illustrated in

Figure 1 on page 5. In this example application (EXTENDED POWER CONFIGURATION), Texas Instruments teaches a voltage doubling circuit comprising:

A diode having an anode and a cathode (as shown);

An inductor (L) connected in series between the diode anode and the power signal (V_I) received from the power connector;

A FET (as shown as a transistor) having a drain and source respectively connected to the diode anode and ground (as shown);

A switching regulator (TL497A) having an input at which the power signal is received (pin 14 of the regulator), and a switched output connected to a gate of the FET (pin 8 of the regulator) at which a FET drive signal is produced to cyclically alternate the polarity across the inductor.

Regarding claim 10, Texas Instruments teaches the additional limitation of a feedback circuit connecting the diode cathode (through resistor R1) to a feedback input of the switching regulator (pin 1 of the TL497A regulator), wherein the switching regulator determines a period of the FET drive signal based on a voltage received at the feedback input.

* * *

Claims 11 – 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lembo in view of Carson et al. (US 5,911,051), Dunlap et al. (US 6,760,799), and Lelong et al. (US Pub. 2004/0033734).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2). .

Regarding claim 11, Lembo teaches an expansion card (page 2, see figure) comprising:

A plurality of Universal Serial Bus (USB) ports adapted to mate with a USB-compatible device (page 2);

A second circuitry for doubling the voltage of the power signal (page 3 of Lembo teaches a "boost converter" to double the 12V power signal to 24V; see note under "Connector Configurations.").

Lembo fails to teach wherein one of the plurality of connectors is an Accelerated Graphics Port (AGP) card connector configured to enable the expansion card to be inserted into an AGP expansion slot of the computer system.

Carson et al. teaches using an Accelerated Graphics Port (AGP) card for the purpose of increasing performance and efficiency through hiding memory access latency, demultiplexing of address and data on the bus, and AC timing (column 4, lines 1 – 11). The system of Carson et al. relates to using AGP for graphics applications. However, Dunlap et al. teach that AGP can also be used for high-volume network traffic (e.g., USB), as well (column 8, line 66 – column 9, line 2).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate an AGP card connector in the expansion card of Lembo for the purpose of improving performance and efficiency.

Lembo, Carson et al., and Dunlap et al. fail to teach a plurality of connectors through which USB data, USB power, and power signals are received, wherein each connector is matable with a corresponding connector of the computer system, and a first circuitry for routing the USB data, USB power and power signals from the plurality of connectors to the USB ports.

Lelong et al. teach a plurality of USB connectors (contained within Figure 2, item 103), through which USB data, USB power and power signals are received, wherein

each connector is matable with a corresponding connector of the computer system (Figure 2, labeled "USB header"; Figure 1, item 15), and a first circuitry for routing the USB data, USB power and power signals from the plurality of connectors to the USB ports (paragraph 39; Figure 2, item 14).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the USB connector as taught by Lelong et al. into the expansion card of Intel Corporation. This would have been obvious in order to allow the USB ports provided on the expansion card to be controlled by a USB host controller incorporated into the computer system motherboard, thus making it unnecessary to include the USB host controller on the expansion card, thus reducing its cost.

Regarding claim 12, Lembo teaches wherein at least one of the plurality of USB ports is a USB-Plus-Power port (page 2) comprising a USB receptacle at which USB data and USB power signals are presented, and a power receptacle at which the power signal is presented (Examiner notes that certain elements in the figure of Lembo may be difficult to discern, and so turns to referencing the Operations Manual of Cyberdata Corporation of the same product. Examiner interprets features shown in the Operations Manual to be inherent in the expansion card as shown in Lembo. Cyberdata Corporation teaches a USB receptacle at which USB data and USB power signals are presented (page 4, pins 1 – 4), and a power receptacle at which the power signal is presented (page 4, pins 5 – 8).

Regarding claim 13, Lelong et al. teach the additional limitation wherein the plurality of connectors further comprises:

A USB connector, matable with a corresponding USB connector of the computer system, at which at least one USB data signal and at least one USB power signal are received (Figure 2, labeled "USB header"; Figure 1, item 15; paragraph 39).

Regarding claim 14, Lelong et al. implicitly teach the additional limitation wherein the plurality of connectors further comprises:

A power connector, matable with a corresponding power connector of the computer system, through which the power signal is received (Examiner notes that, consistent with the USB PlusPower specification, there are four connectors in the conventional USB type-A connector, namely VBUS, GND, Data+ and Data-. Lelong et al. teaches a USB connector (Figure 2, labeled "USB header" and Figure 1, item 15), which, by definition, contains the said four connectors, and therefore contains a power connector (VBUS), thus meeting this limitation).

Regarding claim 15, Lembo teaches the additional limitation wherein the power signal is a 12VDC power signal (page 2, see "Powered-USB PCI Hub Specifications" – Power Output).

Regarding claim 17, Lembo teaches the additional limitation wherein the power signal presented at the power receptacle of at least one of the USB-Plus-Power ports is

a 12VDC power signal (page 3, see "Connector Configurations"), and wherein the second circuitry converts the 12VDC power signal to a 24VDC power signal (where the second circuitry may be interpreted as a boost converter; page 3, see note under "Connector Configurations"),

Wherein the 24VDC power signal is routed to one or more of the at least one USB-Plus-Power ports (page 3, see Connector Configurations; CD#010567A shows Port 1 having the 24VDC power signal).

* * *

Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lembo in view of Carson et al. (US 5,911,051), Dunlap et al. (US 6,760,799), Lelong et al. (US Pub. 2004/0033734), and in view of Texas Instruments.

Regarding claim 18, Lembo, , Carson et al.,Dunlap et al., and Lelong et al. fail to teach the details of the voltage doubling circuit.

Examiner takes official notice that voltage-doubling circuits are old and well known in this art used for the purpose of providing a larger output voltage given a smaller input voltage. This is evidenced by Texas Instruments, where in the TL497A switching voltage regulator specification, an example of an application is illustrated in Figure 1 on page 5. In this example application (EXTENDED POWER CONFIGURATION), Texas Instruments teaches a voltage doubling circuit comprising:

A diode having an anode and a cathode (as shown);

An inductor (L) connected in series between the diode anode and the power signal (V_I) received from the power connector;

A FET (as shown as a transistor) having a drain and source respectively connected to the diode anode and ground (as shown);

A switching regulator (TL497A) having an input at which the power signal is received (pin 14 of the regulator), and a switched output connected to a gate of the FET (pin 8 of the regulator) at which a FET drive signal is produced to cyclically alternate the polarity across the inductor.

Regarding claim 19, Texas Instruments teaches the additional limitation of a feedback circuit connecting the diode cathode (through resistor R1) to a feedback input of the switching regulator (pin 1 of the TL497A regulator), wherein the switching regulator determines a period of the FET drive signal based on a voltage received at the feedback input.

* * *

Claim 16 is rejected under 35 U.S.C. 103(a) as being obvious over Lembo in view of Cyberdata Corporation, Carson et al. (US 5,911,051), Dunlap et al. (US 6,760,799), Lelong et al. (US Pub. 2004/0033734), and further in view of Espenshade et al. (US 6,685,505).

With regard to claim 16, Lembo, Carson et al., Lelong et al., and Dunlap et al. fail to teach the expansion card further comprising at least one circuit each associated with one of the at least one USB port, wherein each circuit performs signal conditioning operations on at least one signal provided at its associated USB port.

Espenshade et al. teach a USB connector that comprises a circuit that performs signal conditioning operations on at least one signal provided at its associated USB port (column 2, lines 9 – 15).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the signal conditioning USB connector of Espenshade et al. in the expansion card of Lembo, Carson et al., Lelong et al., and Dunlap et al. This would have been obvious since Espenshade et al. teach that the signal conditioning components within their USB connector eliminates undesirable extraneous signals such as high frequency noises (column 4, lines 25 – 28).

* * *

Claims 20, 21, and 27 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lembo in view of Carson et al. (US 5,911,051) and Dunlap et al. (US 6,760,799).

Regarding claim 20, Lembo teaches a plurality of connectors (page 2, note four USB ports)for receiving USB data, USB power and power signals, comprising a card

connector (page 2 illustrates a PCI cad connector) configured to enable the expansion card to be inserted into an expansion slot of the computer system (page 2, see figure);

A first Universal Serial Bus (USB)-Plus-Power port (page 2 shows four USB-Plus-Power ports);

A second Universal Serial Bus (USB)-Plus-Power port (page 2 shows four USB-Plus-Power ports);

A doubling circuit (interpreted as a boost converter; page 3, see note under "Connector Configurations"), for doubling the power signal , wherein the power signal is supplied to the first USB-Plus-Power port (page 3, Connector Configurations, CD# 010567A, P2), and the doubled power signal is supplied to the second USB-Plus-Power port (page 3, Connector Configurations, CD# 010567A, P1).

Lembo fails to teach wherein the expansion card uses an Accelerated Graphics Port (AGP) card connector.

Carson et al. teaches using an Accelerated Graphics Port (AGP) card for the purpose of increasing performance and efficiency through hiding memory access latency, demultiplexing of address and data on the bus, and AC timing (column 4, lines 1 – 11). The system of Carson et al. relates to using AGP for graphics applications. However, Dunlap et al. teach that AGP can also be used for high-volume network traffic (e.g., USB), as well (column 8, line 66 – column 9, line 2).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate an AGP card connector in the expansion card of Lembo for the purpose of improving performance and efficiency.

Regarding claim 21, Lembo teaches wherein the first USB-Plus-Power port (page 2) comprises a USB receptacle at which USB data and USB power signals are presented, and a power receptacle at which the power signal is presented (Examiner notes that certain elements in the figure of Lembo may be difficult to discern, and so turns to referencing the Operations Manual of Cyberdata Corporation of the same product. Examiner interprets features shown in the Operations Manual to be inherent in the expansion card as shown in Lembo. Cyberdata Corporation teaches a USB receptacle at which USB data and USB power signals are presented (page 4, pins 1 – 4), and a power receptacle at which the power signal is presented (page 4, pins 5 – 8).

Regarding claim 27, Lembo teaches the additional limitation further comprising a third Universal Serial Bus (USB)-Plus-Power port, wherein the additional power signal is supplied to the third USB-Plus-Power port (Examiner notes there are four USB-Plus-Power ports; page 3, see "Connector Configurations.").

Regarding claim 28, Lembo teaches the additional limitation further comprising a plurality of Universal Serial Bus (USB) ports (page 2, see "Features").

Regarding claim 29, Lembo, Carson et al., and Dunlap et al. fail to explicitly teach a means for routing the USB data, USB power and additional power signals received at the plurality of connectors to the first and second USB-Plus-Power ports.

Examiner takes Official Notice that it would be obvious to one of ordinary skill in this art at the time of invention by applicant to route the USB data, power, and additional power signals received at the plurality of connectors to the first and second USB-Plus-Port ports. This would be obvious in order to make the ports functional, and therefore, useful.

Regarding claim 30, Lembo teaches a second USB-Plus-Power port (page 2; Examiner notes that certain elements in the figure of Lembo may be difficult to discern, and so turns to referencing the Operations Manual of Cyberdata Corporation of the same product. Examiner interprets features shown in the Operations Manual to be inherent in the expansion card as shown in Lembo. Cyberdata Corporation teaches a USB receptacle at which USB data and USB power signals are presented (page 4, pins 1 – 4), and a power receptacle at which the doubled power signal is presented (page 4, pins 5 – 8; page 3, Figure 3; pages 6 – 7, section "Optional +24 Volt Integrated Power Supply).

* * *

Claims 22 – 24, and 26 are rejected under 35 U.S.C. 103(a) as being obvious over Lembo in view of Carson et al. (US 5,911,051), Dunlap et al. (US 6,760,799), and further in view of Lelong et al. (US Pub. 2004/0033734).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2). .

With regard to claim 22, Lembo, Cyberdata Corporation, Carson et al., and Dunlap et al. fail to teach a USB connector, matable with a corresponding USB connector of the computer system, at which at least one additional USB data signal and at least one USB power signal generated by the computer system are received, wherein each of the additional USB data signal and USB power signal is routed to one or more of the at least one USB port.

Lelong et al. teach a USB connector (Figure 2, item 103), matable with a corresponding USB connector of the computer system (Figure 2, labeled "USB header";

Figure 1, item 15), at which at least one additional USB data signal and at least one USB power signal generated by the computer system are received, wherein each of the additional USB data signal and USB power signal is routed to one or more of the at least one USB port (paragraph 39).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the USB connector as taught by Lelong et al. into the expansion card of Intel Corporation. This would have been obvious in order to allow the USB ports provided on the expansion card to be controlled by a USB host controller incorporated into the computer system motherboard, thus making it unnecessary to include the USB host controller on the expansion card, thus reducing its cost.

Regarding claim 23, Lelong et al. implicitly teach the additional limitation wherein the plurality of connectors further comprises:

A power connector, matable with a corresponding power connector of the computer system, through which the power signal is received (Examiner notes that, consistent with the USB PlusPower specification, there are four connectors in the conventional USB type-A connector, namely VBUS, GND, Data+ and Data-. Lelong et al. teaches a USB connector (Figure 2, labeled "USB header" and Figure 1, item 15), which, by definition, contains the said four connectors, and therefore contains a power connector (VBUS), thus meeting this limitation).

Regarding claim 24, Lembo teaches the additional limitation wherein the power signal is a 12VDC power signal (page 2).

Regarding claim 26, Lembo teaches the additional limitation wherein the doubling circuit converts the 12VDC power signal to a 24VDC power signal (where the doubling circuit is interpreted as a boost converter; page 3, see note under "Connector Configurations."),

Wherein the 24VDC power signal is routed to the second USB-Plus-Power port (page 3, see "Connector Configurations"; CD#010567A shows Port 1 having the 24VDC power signal).

* * *

Claim 25 is rejected under 35 U.S.C. 103(a) as being obvious over Lembo in view of Carson et al. (US 5,911,051), Dunlap et al. (US 6,760,799), Lelong et al. (US Pub. 2004/0033734), and further in view of Espenshade et al. (US 6,685,505).

With regard to claim 25, Lembo, Carson et al., Lelong et al., Dunlap et al., and Lelong et al. fail to teach the expansion card further comprising at least one circuit each associated with one of the at least one USB port, wherein each circuit performs signal conditioning operations on at least one signal provided at its associated USB port.

Espenshade et al. teach a USB connector that comprises a circuit that performs signal conditioning operations on at least one signal provided at its associated USB port (column 2, lines 9 – 15).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the signal conditioning USB connector of Espenshade et al. in the expansion card of Lembo, Carson et al., Lelong et al., Dunlap et al., and Lelong et al. This would have been obvious since Espenshade et al. teach that the signal conditioning components within their USB connector eliminates undesirable extraneous signals such as high frequency noises (column 4, lines 25 – 28).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MDS

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100